ON Semiconductor®

P2042A

LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 15dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- Input frequency range: 30MHz -110MHz.
- Output frequency range: 30MHz -110MHz
- Optimized for 32.5MHz, 54MHz, 65MHz, 74MHz and 108MHz pixel clock frequencies
- Internal loop filter minimizes external components and board space
- Eight selectable high spread ranges up to ±2%
- Selectable Center Spread options
- SSON# control pin for spread spectrum enable and disable options
- Low cycle-to-cycle jitter
- 3.3V ± 0.3V operating range
- CMOS design
- Supports most mobile graphic accelerator and LCD timing controller specifications
- Available in 8-pin TSSOP Package

Product Description

The P2042A is a versatile spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2042A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2042A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

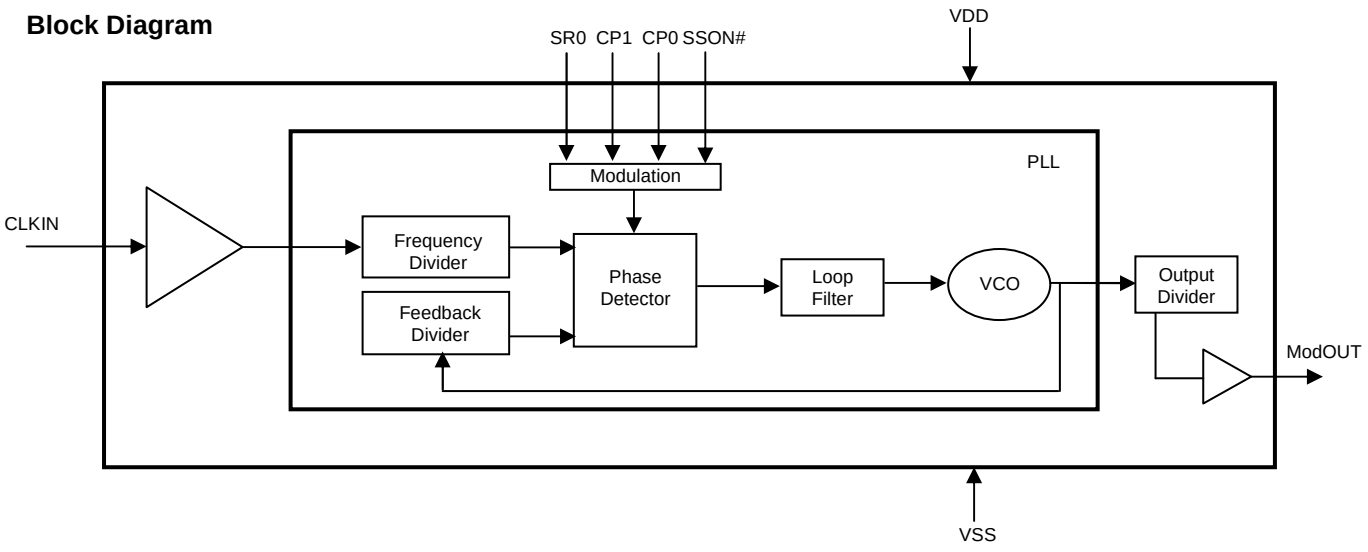
The P2042A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2042A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

Applications

The P2042A is targeted towards digital flat panel applications for notebook PCs, palm-size PCs, office automation equipments and LCD monitors.

Block Diagram



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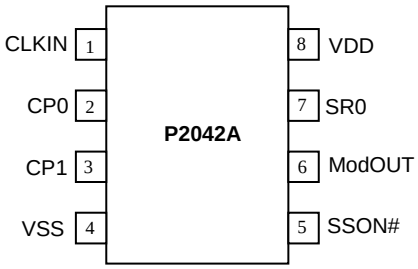
Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	CP0	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor. Refer to *Modulation Selection Table.*
3	CP1	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor. Refer to *Modulation Selection Table.*
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor. Refer to *Modulation Selection Table.*
8	VDD	P	Power supply for the entire chip.

Modulation Selection

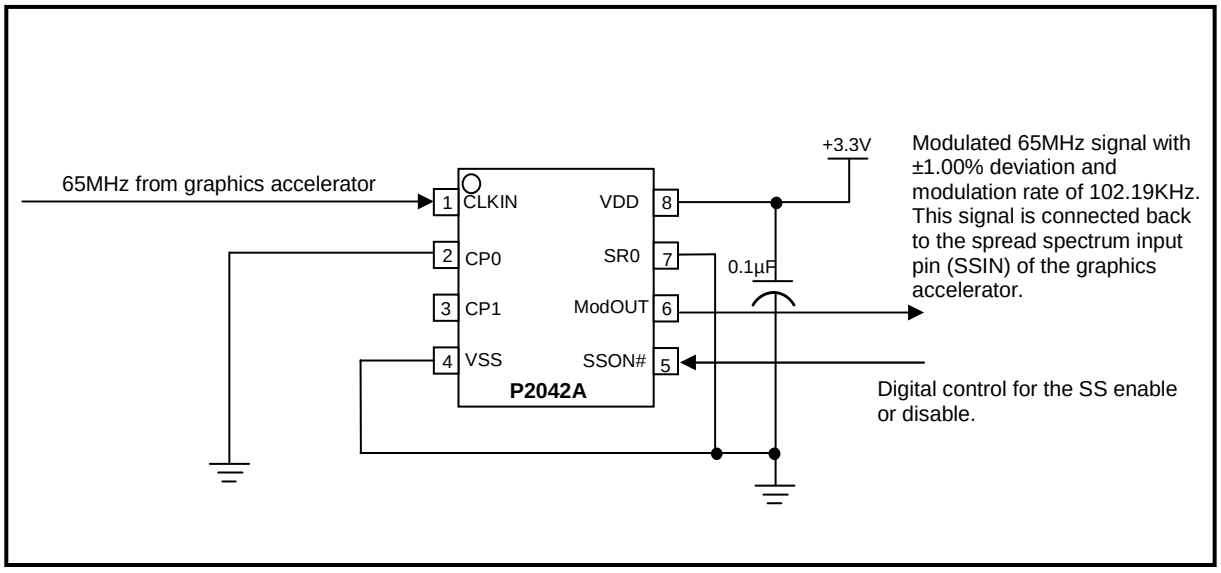
CP0	CP1	SR0	Spreading Range (± %)					Modulation Rate (KHz)
			32.5MHz	54MHz	65MHz	81MHz	108MHz	
0	0	0	1.75	1.53	1.41	1.27	1.1	(FIN /40) * 62.89 KHz
0	0	1	1.89	1.7	1.55	1.4	1.2	
0	1	0	1.39	1.2	1.1	1.0	0.9	
0	1	1	2.1	1.85	1.7	1.55	1.35	
1	0	0	0.74	0.6	0.57	0.52	0.45	
1	0	1	1.1	0.93	0.86	0.77	0.68	
1	1	0	0.32	0.3	0.28	0.26	0.23	
1	1	1	0.58	0.5	0.45	0.4	0.36	

Spread Spectrum Selection

The *Modulation Selection Table* defines the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency. (Note: The center frequency is the frequency of the external reference input on CLKIN, pin1).

For example, P2042A is designed for high-resolution, flat panel applications and is able to support an XGA (1024 x 768) flat panel operating at 65MHz (FIN) clock speed. A spreading selection of CP0=0, CP1=1 and SR0=0 provides a percentage deviation of ±1.00% from F_{IN}. This results in the frequency on ModOUT being swept from 65.65 to 64.35MHz at a modulation rate of 102.19KHz. Refer to *Modulation Selection Table*. The example in the following illustration is a common EMI reduction method for a notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

Application Schematic for Mobile LCD Graphics Controllers



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter			Min	Typ	Max	Unit
VDD	Supply Voltage with respect to Ground			3.0	3.3	3.6	V
T_A	Operating temperature	Commercial		0		+70	℃
T_J	Junction temperature	Commercial	TSSOP			79.80	℃
θ_{JC}	Thermal Resistance	TSSOP			124		℃/W

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS - 0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD + 0.3	V
I_{IL}	Input low current (pull-up resistor on inputs CP0, CP1 and SR0)			-50	µA
I_{IH}	Input high current (pull-down resistor on input SSON#)			50	µA
V_{OL}	Output low voltage (I_{OL} = 8mA)			0.4	V
V_{OH}	Output high voltage (I_{OH} = -8mA)	2.5			V
I_{DD}	Static supply current (CLKIN pulled LOW)			300	µA
I_{CC}	Dynamic supply current (3.3V and 10pF loading)	6	15	22	mA
V_{DD}	Operating voltage	3.0	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power up)			3	mS
Z_{OUT}	Clock output impedance		35		Ω

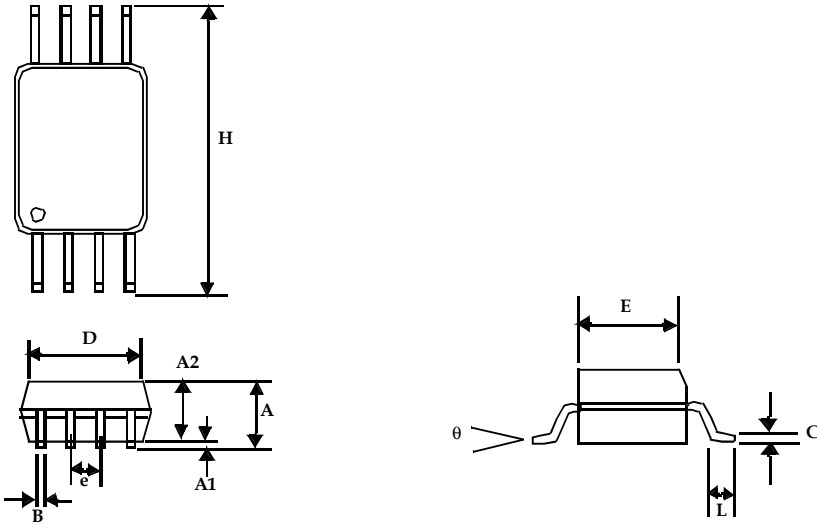
AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input Clock frequency		30	74	110	MHz
f_{OUT}	Output Clock frequency		30	74	110	MHz
t_{LH}[1]	Output rise time (measured between 20% to 80%)		1.1	1.5	2	nS
t_{HL}[1]	Output fall time (measured between 80% to 20%)		0.8	1.2	1.8	nS
t_{JC}	Jitter (cycle-to-cycle)	<50MHz			±250	pS
		≥50MHz			±200	
t_D	Output duty cycle		45	50	55	%

Note: 1. t_{LH} and t_{HL} are measured into a capacitive load of 10pF

Package Information

8-lead TSSOP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Ordering Information

Part Number	Top Marking	Package Type	Temperature
P2042AF-08TR	P2042AF	8-Pin TSSOP, TAPE & REEL, Green	0℃ to +70℃

Note: Many ON Semiconductor products are protected by issued patents or applications for patent.

PUBLICATION ORDERING INFORMATION

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